GS1528A and GS9068A

HD-LINX® II Multi-Rate Dual Slew-Rate Cable Driver

Features

GS1528A

- SMPTE 292M, SMPTE 344M and SMPTE 259M compliant
- Dual coaxial cable driving outputs with selectable slew rate
- 50Ω differential PECL input
- Pb-free and RoHS compliant
- Pin compatible with GS9068A HD-LINX II SD SDI cable driver
- Seamless interface to other HD-LINX II family products
- Single 3.3V power supply operation
- Operating temperature range: 0°C to 70°C

GS9068A

- SMPTE 259M and SMPTE 344M compliant
- Dual coaxial cable driving outputs
- 50W differential PECL input
- Pb-free and RoHS compliant
- Pin compatible with GS1528A HD-LINX II multi-rate SDI dual slew-rate cable driver
- Seamless interface to other HD-LINX II family products
- Single 3.3V power supply operation
- Operating temperature range: 0°C to 70°C

Applications

GS1528A

- SMPTE 292M, SMPTE 344M and SMPTE 259M Coaxial Cable Serial Digital Interfaces

GS9068A

- SMPTE 259M and SMPTE 344M Coaxial Cable Serial Digital Interfaces

Description

The GS1528A/9068A is a second generation, high speed BiCMOS integrated circuit designed to drive one or two 75W coaxial cables.

The GS1528A may drive data rates up to 1.485Gb/s and provides two selectable slew rates in order to achieve compliance to SMPTE 259M, SMPTE 344M and SMPTE 292M.

The GS9068A may drive data rates up to 540Mb/s and will achieve compliance to SMPTE 259M and SMPTE 344M.

The GS1528A/9068A accepts a LVPECL level differential input that may be AC coupled. External biasing resistors at the inputs are not required. Power consumption is typically 168mW using a 3.3V power supply. The GS1528A/9068A is Pb-free, and the encapsulation compound does not contain halogenated flame retardant. This component and all homogeneous sub components are RoHS compliant.

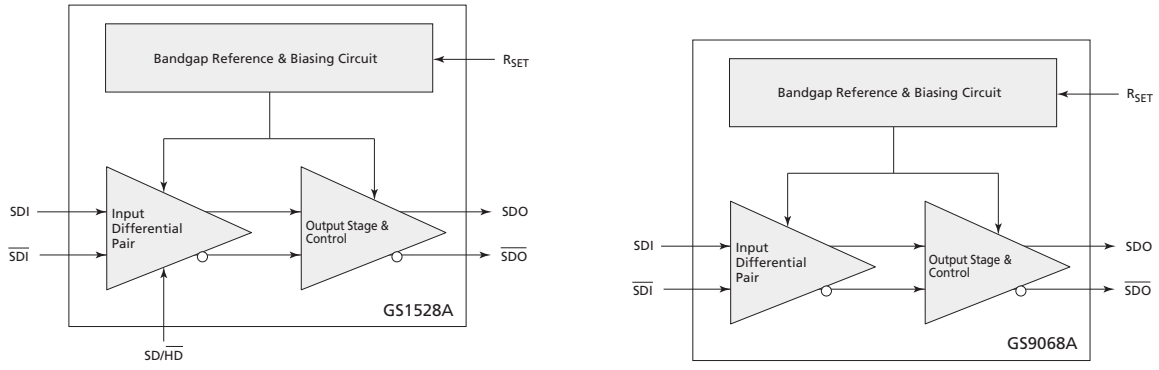


Figure A: GS1528A (left) and GS9068A (right) Functional Block Diagrams

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
7	158377	–	July 2012	Correction in GS9068A Pin Assignment
6	154747	–	August 2010	Correction to Package Dimensions and Ordering Information.
5	153754	–	November 2009	Updated to latest Gennum template.
4	139112	38124	January 2006	Corrected Input Differential Swing to 2200mV.
3	137886	–	September 2005	Corrected process to BiCMOS.
2	137403	–	July 2005	Updated to current document template to remove "Proprietary and Confidential" footer. Re-ordered solder reflow profiles to show preference for Pb-free profile. Clarified naming of standard Pb solder reflow profile. Added packaging data section. Updated document to reflect the RoHS compliance of both the GS1528A and GS9068A.
1	133654	–	June 2004	Modified Table 2-3. Added reflow profiles. Upgraded from a preliminary data sheet to a data sheet.
0	132954	–	February 2004	New document.

Contents

1. Pin Out

1.1 GS1528A Pin Assignment

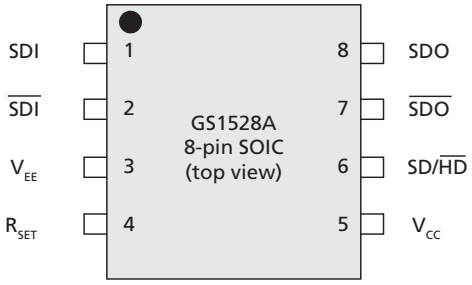


Figure 1-1: 8 Pin SOIC

1.2 GS9068A Pin Assignment

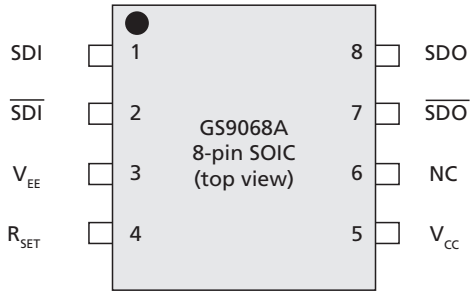


Figure 1-2: 8 Pin SOIC

1.3 GS1528A/GS9068A Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
1,2	SDI, $\overline{SDI}$	Analog	Input	Serial digital differential input.
3	V_{EE}	–	Power	Most negative power supply connection. Connect to GND.
4	R_{SET}	Analog	Input	External output amplitude control resistor.
5	V_{CC}	–	Power	Most positive power supply connection. Connect to +3.3V.
6	SD/$\overline{HD}$	Non Synchronous	Input	GS1528A: Output slew rate control. When set HIGH, the output will meet SMPTE 259M rise/fall time specifications. When set LOW, the serial outputs will meet SMPTE 292M rise/fall time specifications.
	NC	–	–	GS9068A: No connect. Not connected internally.
7, 8	$\overline{SDO}$, SDO	Analog	Output	Serial digital differential output.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1 lists the absolute maximum ratings for the GS1528A/GS9068A. Conditions exceeding the limits listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5V to 3.6 V_{DC}
Input ESD Voltage	2kV
Storage Temperature Range	-50°C < T_s < 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V
Operating Temperature Range	0°C to 70°C
Solder Reflow Temperature	260°C
Power Dissipation	300mW

2.2 DC Electrical Characteristics

Table 2-2 shows the DC electrical characteristics of the GS1528A and the GS9068A where conditions are V_{DD} = 3.3V, T_A = 0°C to 70°C, unless otherwise specified.

Table 2-2: DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes	Test Levels
Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V	±5%	3
Power Consumption	P_D	T_A = 25°C	–	168	–	mW	–	5
Supply Current	I_s	T_A = 25°C	–	51	64	mA	–	1
Output Voltage	V_{CMOUT}	Common mode	–	V_{CC} - V_{OUT}	–	V	–	6
Input Voltage	V_{CMIN}	Common mode	1.6 + $\Delta V_{SDI}/2$	–	V_{CC} - $\Delta V_{SDI}/2$	V	–	6

Table 2-2: DC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes	Test Levels
SD/$\overline{HD}$ Input	V_{IH}	–	2.4	–	–	V	1	7
	V_{IL}	–	–	–	0.8	V	1	7

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guard bands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guard bands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES:

1. This parameter applies only to the GS1528A.

2.3 AC Electrical Characteristics

Table 2-3 shows the AC electrical characteristics of the GS1528A and the GS9068A where conditions are V_{DD} = 3.3V, T_A = 0°C to 70°C, unless otherwise specified.

Table 2-3: AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes	Test Levels
Serial input data rate	DR_{SDO}	GS1528A	–	–	1.485	Gb/s	1	1
	DR_{SDO}	GS9068A	–	–	540	Mb/s	–	1
Additive jitter	–	1.485Gb/s	–	22	–	ps_{p-p}	2	1
	–	270Mb/s	–	16	–	ps_{p-p}	–	4
	–	GS9068A	–	16	–	ps_{p-p}	–	1
Rise/Fall time	t_r, t_f	SD/$\overline{HD}$=0	–	–	220	ps	2, 3	1
	t_r, t_f	SD/$\overline{HD}$=1	400	–	800	ps	2, 3	1
	t_r, t_f	GS9068A	400	–	800	ps	3	1
Mismatch in rise/fall time	$\triangle t_r$, $\triangle t_f$	–	–	–	30	ps	–	1
Duty cycle distortion	–	SD/$\overline{HD}$=0	–	–	30	ps	2	1
	–	SD/$\overline{HD}$=1	–	–	100	ps	2	7
	–	GS9068A	–	–	100	ps	–	1

Table 2-3: AC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes	Test Levels
Overshoot	–	SD/$\overline{HD}$=0	–	–	10	%	2	7
	–	SD/$\overline{HD}$=1	–	–	8	%	2	1
	–	GS9068A	–	–	8	%	–	1
Output Return Loss	ORL	–	15	–	–	dB	–	7
Output Voltage Swing	V_{OUT}	Single Ended into 75Ω external load R_{SET} = 750Ω	750	800	850	mV_{p-p}	–	1
Input Voltage Swing	$\triangle V_{SDI}$	Differential	300	–	2000	mV_{p-p}	–	7

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guard bands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guard bands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES:

1. The input coupling capacitor must be set accordingly for lower data rates.
2. This parameter applies only to the GS1528A.
3. Rise/Fall time measured between 20% and 80%.

3. Solder Reflow Profile

The maximum Pb-free reflow profile is shown in Figure 3-1.

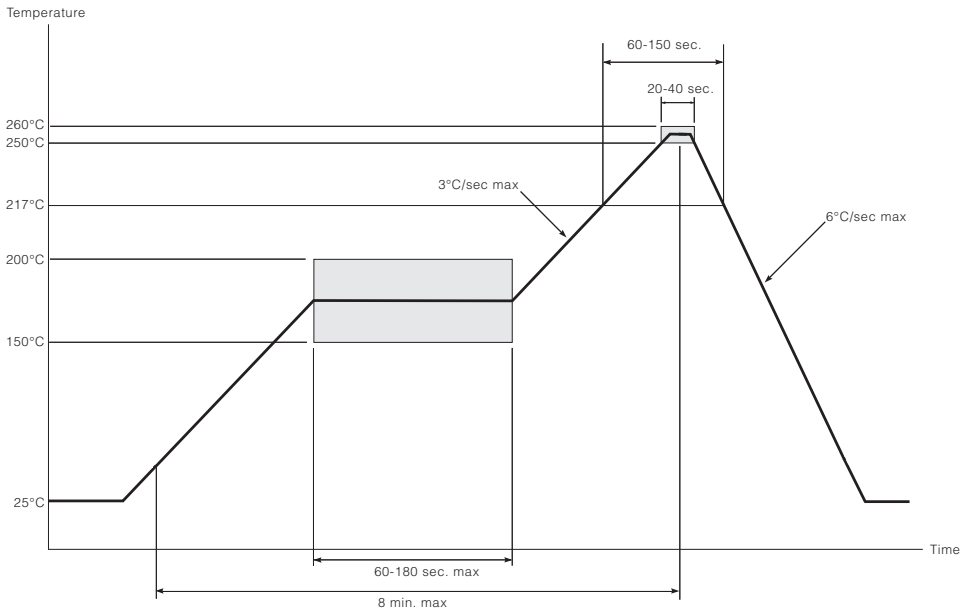


Figure 3-1: Maximum Pb-free Solder Reflow Profile

4. Input / Output Circuits

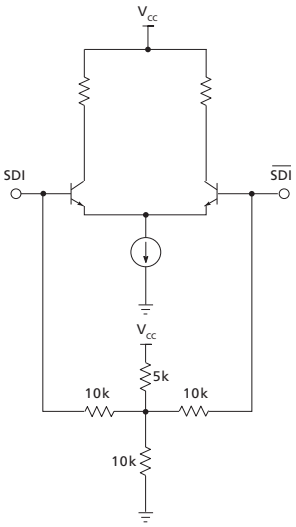


Figure 4-1: Differential Input Stage (SDI/$\overline{SDI}$)

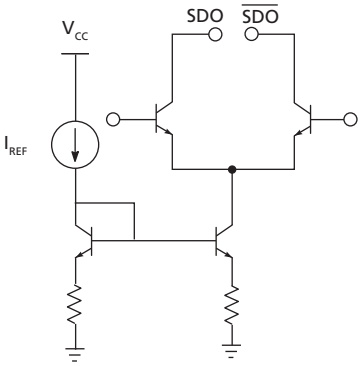


Figure 4-2: Differential Output Stage (SDO/$\overline{SDO}$) I_{REF} derived using R_{SET}

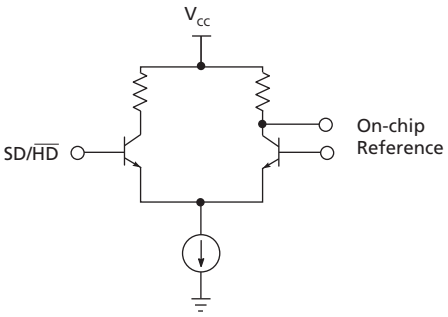


Figure 4-3: Slew Rate Select Input Stage (GS1528A only)

5. Detailed Description

5.1 Input Interfacing

SDI/$\overline{\text{SDI}}$ are high impedance differential inputs. The equivalent input circuit is shown in Figure 4-1.

Several conditions must be observed when interfacing to these inputs:

- The differential input signal amplitude must be between 300 and 2000mVp-p.
- The common mode voltage range must be as specified in Table 2.2.
- For input trace lengths longer than approximately 1cm, the inputs should be terminated as shown in the Typical Application Circuit.

The GS1528A/9068A inputs are self-biased, allowing for simple AC coupling to the device. For serial digital video, a minimum capacitor value of 4.7µF should be used to allow coupling of pathological test signals. A tantalum capacitor is recommended.

SD/$\overline{\text{HD}}$ Input Pin (GS1528A only):

The GS1528A SDO rise and fall times can be set to comply with both SMPTE 259M/344M and SMPTE 292M. For all SMPTE 259M standards, or any data rate that requires longer rise and fall time characteristics, the SD/$\overline{\text{HD}}$ pin must be set HIGH by the application layer. For SMPTE 292M standards and signals which require faster rise and fall times, this pin should be set LOW.

5.2 Output Interfacing

The GS1528A/9068A outputs are current mode, and will drive 800mV into a 75Ω load. These outputs are protected from accidental static damage with internal static protection diodes.

The SMPTE 292M, SMPTE 344M and SMPTE 259M standards require that the output of a cable driver have a source impedance of 75Ω and a return loss of at least 15dB between 5MHz and 1.485GHz.

In order for an SDI output circuit using the GS1528A/9068A to meet this specification, the output application circuit shown in Typical Application Circuits on page 14 is recommended.

The value of L_{COMP} will vary depending on the PCB layout, with a typical value of 5.6nH. A 4.7µF capacitor is used for AC-coupling the output of the device. This value is chosen to ensure that pathological signals can be coupled without a significant DC component occurring. Please see Application Information on page 14 for more details.

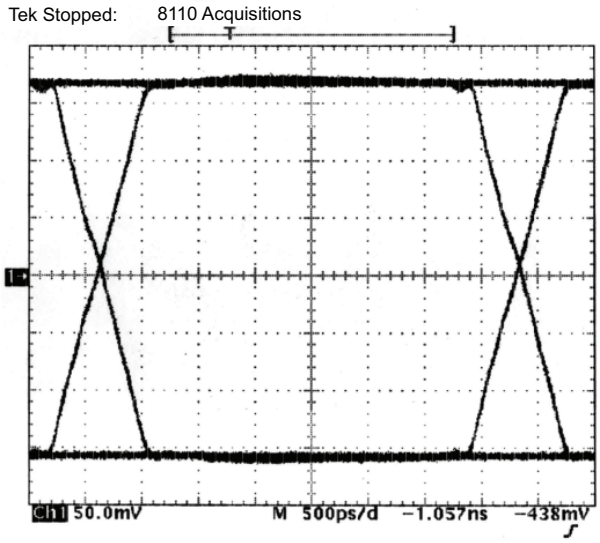


Figure 5-1: Output signal for 270Mb/s input

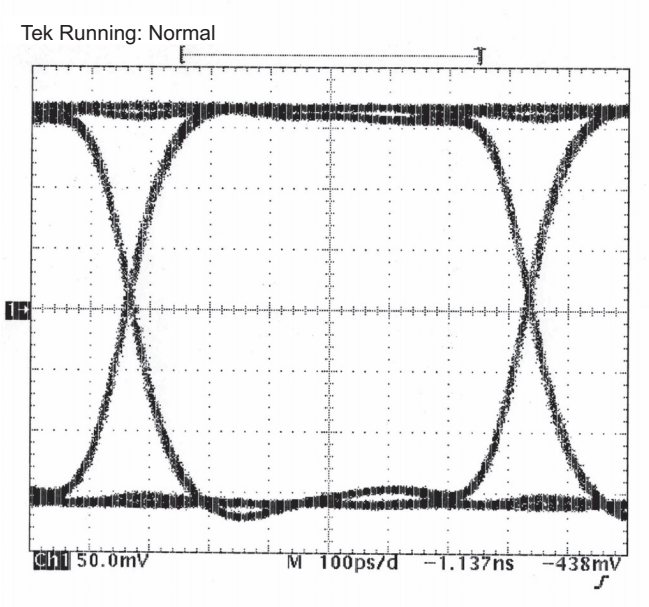


Figure 5-2: Output signal for 1.485Gb/s input (GS1528A only)

The output protection diodes act as a varactor (voltage controlled capacitor) as shown in Figure 5-3. Therefore, when measuring return loss at the GS1528A/9068A output, it is necessary to take the measurement for both a logic high and a logic low output condition.

Consequently, the output capacitance of the device is dependent on the logic state of the output.

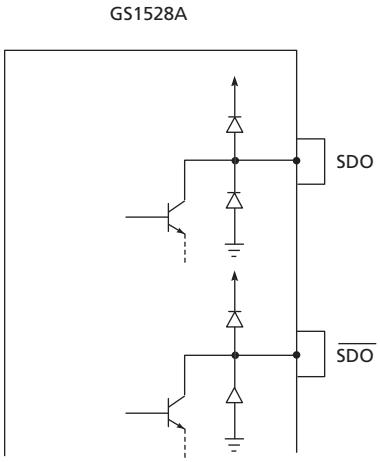


Figure 5-3: Static Protection Diodes

5.3 Output Return Loss Measurement

To perform a practical return loss measurement, it is necessary to force the GS1528A/9068A output to a DC high or low condition. The actual measured return loss will be based on the outputs being static at V_{CC} or V_{CC}-1.6V. Under normal operating conditions the outputs of the device swing between V_{CC}-0.4V and V_{CC}-1.2V, so the measured value of return loss will not represent the actual operating return loss.

A simple method of calculating the values of actual operating return loss is to interpolate the two return loss measurements. In this way, the values of return loss are estimated at V_{CC}-0.4V and V_{CC}-1.2V based on the measurements at V_{CC} and V_{CC}-1.6V.

The two values of return loss (high and low) will typically differ by several decibels. If the measured return loss is R_H for logic high and R_L for logic low, then the two values can be interpolated as follows:

$R_{IH} = R_H - (R_H - R_L)/4$ and

$R_{IL} = R_L + (R_H - R_L)/4$

Where R_{IH} is the interpolated logic high value and R_{IL} is the interpolated logic low value.

For example: if R_H = -18dB and R_L = -14dB, then the interpolated values are R_{IH} = -17dB and R_{IL} = -15dB.

5.4 Output Amplitude Adjustment

The output amplitude of the GS1528A/9068A can be adjusted by changing the value of the R_{SET} resistor as shown in Table 5-1. For an 800mV_{p-p} output with a nominal ±7% tolerance, a value of 750Ω is required. A ±1% SMT resistor should be used.

The R_{SET} resistor is part of the high speed output circuit of the GS1528A/9068A. The resistor should be placed as close as possible to the R_{SET} pin. In addition, the PCB capacitance should be minimized at this node by removing the PCB groundplane beneath the R_{SET} resistor and the R_{SET} pin.

Table 5-1: R_{SET} vs V_{OD}

R_{SET} Resistance (Ω)	Output Swing (mVp-p)
995	608
824	734
750	800
680	884
573	1040

NOTE: For reliable operation of the GS1528A/9068A over the full temperature range, do not use an R_{SET} value below 573Ω.

6. Application Information

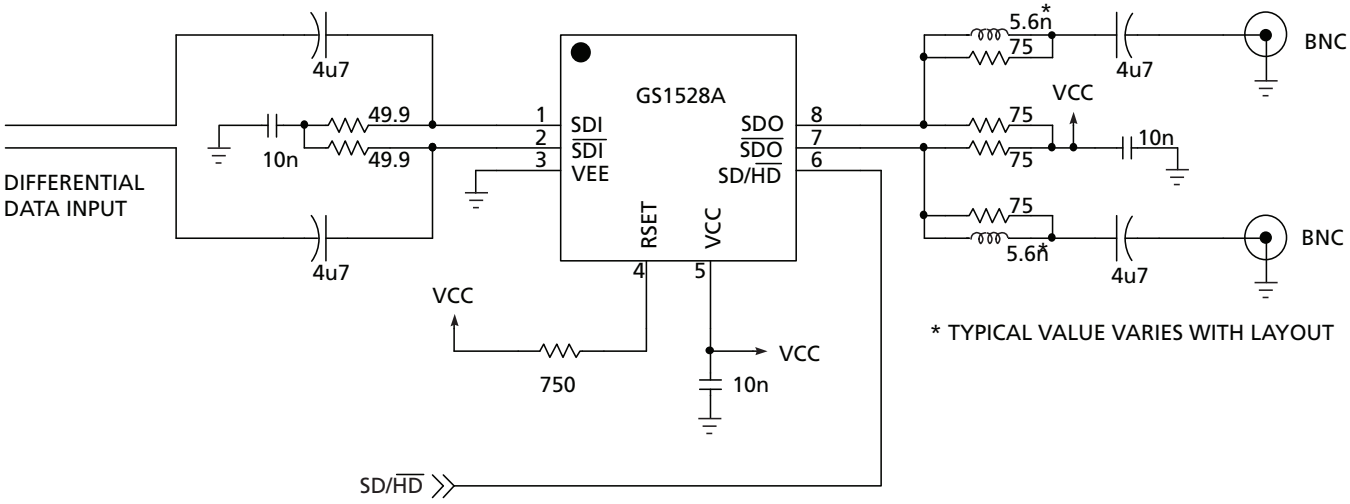
6.1 PCB Layout

Special attention must be paid to component layout when designing serial digital interfaces for HDTV.

An FR-4 dielectric can be used, however, controlled-impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

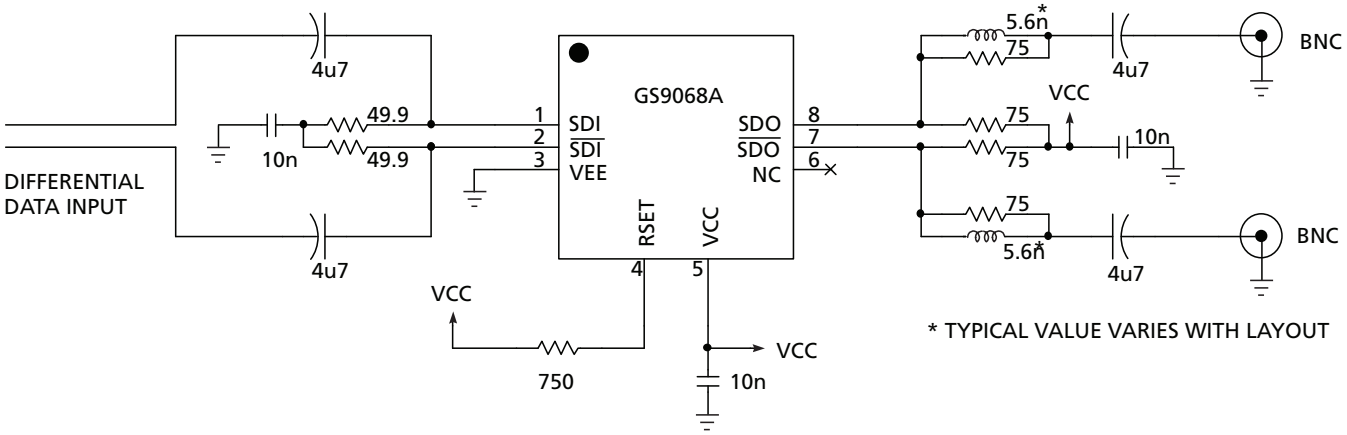
- The PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to changes in trace impedance
- The PCB groundplane is removed under the GS1528A/9068A output components to minimize parasitic capacitance
- The PCB ground plane is removed under the GS1528A/9068A R_{SET} pin and resistor to minimize parasitic capacitance
- Input and output BNC connectors are surface-mounted in-line to eliminate a transmission line stub caused by a BNC mounting via high-speed traces, which are curved to minimize impedance variations due to change of PCB trace width

6.2 Typical Application Circuits



NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise noted.

Figure 6-1: GS1528A Typical Application Circuit

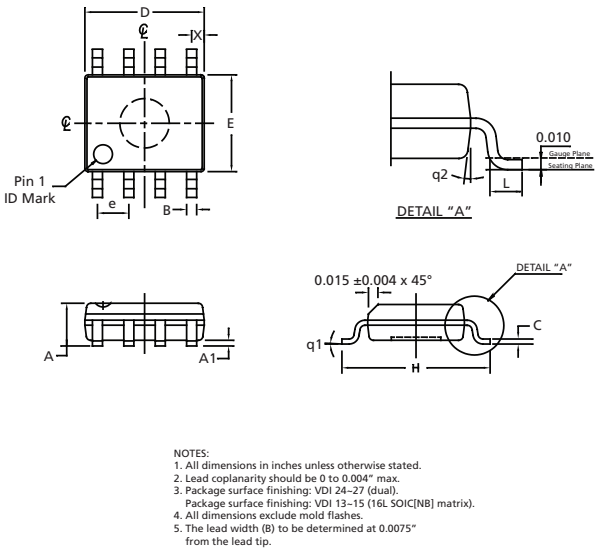


NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise noted.

Figure 6-2: GS9068A Typical Application Circuit

7. Package & Ordering Information

7.1 Package Dimensions



SYMBOL	8 SOIC	
	Min.	Max.
A	0.054	0.068
A1	0.004	0.0098
B	0.014	0.019
D	0.189	0.196
E	0.150	0.157
H	0.229	0.244
e	0.050 BSC	
C	0.0075	0.0098
L	0.016	0.034
X	0.0215 REF	
q1	0°	8°
q2	7° BSC	

NOTES:
1. All dimensions in inches unless otherwise stated.
2. Lead coplanarity should be 0 to 0.004" max.
3. Package surface finishing: VDI 24–27 (dual).
   Package surface finishing: VDI 13–15 (16L SOIC[NB] matrix).
4. All dimensions exclude mold flashes.
5. The lead width (B) to be determined at 0.0075"
   from the lead tip.

7.2 Packaging Data

Table 7-1: Packaging Data

Parameter	Value
Package Type	8-pin SOIC
Moisture Sensitivity Level	2
Junction to Case Thermal Resistance, θ_{j-c}	72°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	116°C/W
Pb-free and RoHS Compliant	Yes

7.3 Ordering Information

Table 7-2: Ordering Information

Product	Part Number	Package	Temperature Range
GS1528A	GS1528ACKAE3	8-pin SOIC	0°C to 70°C
GS1528A	GS1528ACTAE3	8-pin SOIC, 250pc tape and reel	0°C to 70°C
GS1528A	GS1528ACTAE3D	8-pin SOIC, 500pc tape and reel	0°C to 70°C
GS9068A	GS9068ACKAE3	8-pin SOIC	0°C to 70°C
GS9068A	GS9068ACTAE3	8-pin SOIC, 250pc tape and reel	0°C to 70°C

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